REMARKS

This responds to the Office Action mailed on July 22, 2004.

Claims 1, 8, 15, 20, 24, 31, 32, 33, and 34 are amended, no claims are canceled, and no claims are added; as a result, claims 1-35 are now pending in this application.

Request for Telephonic Interview

Applicants' counsel, Sherry W. Schumm, respectfully requests a telephonic interview to discuss how the present claim amendments distinguish over IEEE 1364. The Examiner is requested to contact Applicants' counsel at 480-657-3766 to schedule a time for the interview.

§102 Rejection of the Claims

Claims 1-8, 12-30, and 33 were rejected under 35 USC § 102(b) as being anticipated by IEEE Std 1364-1995 – IEEE Standard Hardware Description Language Based on the Verilog® Hardware Description Language (herein "IEEE 1364"). Applicant respectfully traverses the rejection.

Applicant has amended claims 1, 8, 15, 20, 24, and 33, from which claims 12-14, 16-19, 21-23, and 25-30 depend, respectively, to clarify arrangements of the claim elements. Applicant's first ground of traverse rests on the fact that IEEE 1364 does not include Applicant's claim elements arranged as set forth in the claims. "Anticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim*." *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added).

IEEE 1364 describes various definitions relating to Verilog HDL. However, IEEE 1364 does not describe the arrangements of processes, apparatus, or means elements claimed in the present application. Applicant respectfully requests that the Examiner provide citations in IEEE 1364 showing Applicant's claim elements arranged as they are set forth in the claims.

Additionally, Applicant submits that IEEE 1364 does not teach each end every claim element of claims 1-8, 12-30, and 33 arranged as they are in the claims. Applicant's claims are

distinguishable from IEEE 1364 in that Applicant's claims include at least the following distinguishing language:

- A method or at least one simulation or behavior module, which performs the functions of

  forcing (or conveying) an initial forced logic state (or initial node condition) on the node of a simulated circuit,

  after forcing (or conveying), releasing the node from the initial forced logic state (or initial node condition),

  monitoring the node after the node has been released, and

  providing (or outputting) an indication, in response to the monitoring, when the node is in a preselected condition (or an undesirable state).

  (claims 1-8, 12-23, 33)

- a system comprising a circuit module, which when executed

  a conveying means for conveying an initial node condition to a simulated circuit node,

  a release means for releasing the initial node condition, wherein releasing the initial node condition occurs after conveying,

  a monitoring means for monitoring the simulated circuit node for a node condition after releasing the initial node condition, and

  a first output means for outputting an indication when the node condition is in an undesirable state, in response to the monitoring.

  (claim 24)

- an HDL module comprising

  a means for maintaining a logic level of a simulated circuit node until a release condition is met, wherein . . . a simulation program is able to change a logic state of the simulated circuit node after the release condition is met.

(claims 25-27)

- an HDL module comprising

an initial condition release means, which enables a simulation program to change a logic state of a simulated circuit node after a release condition is met.

(claim 28)

- an HDL module comprising

means for maintaining a logic level of a simulated circuit node for a predetermined period of time, and

means for releasing an initial condition after a release condition is met, wherein releasing the initial condition enables a simulation program to change the logic level of the simulated circuit node, and wherein the predetermined period of time is a simulation run time defined by an HDL simulation executable program.

(claims 29, 30)

Based on the claim amendments and the reasons explained above, Applicant believes that IEEE 1364 does not disclose the features of Applicant's claims 1-8, 12-30, and 33. Accordingly, Applicant believes that these claims are in a condition for allowance. Applicant respectfully requests that the Examiner reconsider and withdraw the rejection in light of Applicant's amendments and remarks.

§103 Rejection of the Claims

Claims 9-11, 31, 32, 34, and 35 were rejected under 35 USC § 103(a) as being unpatentable over IEEE in view of Official Notice. Applicant respectfully traverses the rejection.

Claims 9-11:

Claims 9-11 are dependent from claim 8, which was rejected in the Office Action under 35 U.S.C. § 102. As discussed above in response to the rejection of claim 8, Applicant believes that claim 8 (and thus claims 9-11) is distinguishable over IEEE 1364, and more specifically, that IEEE 1364 does not disclose the features of claim 8 in the arrangement claimed. Applicant

further believes that IEEE 1364 neither discloses, suggests, nor motivates the limitations of Applicant's claims 9-11 in the arrangement claimed.

The Office Action, on page 23, gives support to its previous Official Notice that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features detailed above as to enable re-forcing a node's value if testing indicates that a node's value is unknown, because it is impossible to do analysis on a node with an unknown value." Particularly, the Office Action cites IEEE Std 1164-1993: Multivalue Logic System for VHDL Model Interoperability, pp. 4-5. This reference includes various truth tables, which indicate various gate output values for various inputs. Applicant disagrees that these truth tables relate to forcing or re-forcing a node condition. They are merely tables indicating inputs and outputs to gates.

Further, The Office Action states, on page 23, that "the VHDL language is a direct competitor to the Verilog language, and provides almost the same functionality as the Verilog language." Applicant believes that the combination of IEEE 1364-1995 and IEEE 1164-1993 is erroneous for this and other reasons. First, if the languages are competitors, there would be no motivation to combine and, in fact, there would be a motivation away from combining the two languages, because they are incompatible and use different syntaxes. In addition, no suggestion or motivation to combine these references can be found in the references themselves.

Regarding the Official Notice that ". . . it is preferable to do analysis on a node that has a derived value as opposed to one with an arbitrarily assigned value," Applicant believes that the same arguments apply as presented in the immediately paragraphs, and that there is a motivation away from combining the references.

Still further, IEEE 1364-1995 and IEEE 1164-1993, either singularly or in combination, do not teach or suggest all the features of claims 9-11, particularly the arrangement of the features in these claims. Accordingly, Applicant believes that claims 9-11 are in a condition for allowance, and respectfully requests that the Examiner reconsider and withdraw the rejection of claims 9-11.

Claims 31 and 32:

The Office Action, on page 24, gives support to its previous Official Notice that ". . . it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a circuit with a known state pass on its state to a linked circuit with an unknown state, because this represents the propagation of a signal in a circuit." Particularly, the Office Action again relies on IEEE Std. 1164-1993 to provide this support. As described in the immediately preceding paragraphs regarding claims 9-11, Applicant believes that, not only is there no motivation to combine IEEE 1164-1993 and IEEE 1364-1995, but there is a motivation away from combining these references. Further, IEEE 1364-1995 and IEEE 1164-1993, either singularly or in combination, do not teach or suggest all the features of claims 31 and 32, particularly the arrangement of the features in these claims.

Also, regarding claims 31 and 32, previous Official Notice was given that ". . . it would have been obvious to one of ordinary skill in the art at the time the invention was made to create two (or three) modules, because some simple circuits have only two (or three) components of interest." Claims 31 and 32 include "HDL modules" and not circuit components. Accordingly, Applicant believes that the given Official Notice does not accurately apply to claims 31 and 32. Applicant requests clarification, if the rejection on this basis is repeated.

For the reasons given above, Applicant believes that claims 31 and 32 are in a condition for allowance, and respectfully requests that the Examiner reconsider and withdraw the rejection of claims 31 and 32.

Claims 34 and 35:

The Office Action, on pages 23-25, gives support to its previous Official Notices regarding claim 34 (from which claim 35 depends). In conjunction with Applicant's remarks regarding the rejection of claims 9-11 under 35 USC § 103(a), Applicant discussed the Official Notices that ". . . it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features detailed above as to enable re-forcing a node's value if testing indicates that a node's value is unknown, because it is impossible to do analysis on a node with an unknown value," and that ". . . it is preferable to do analysis on a node that has a derived value as opposed to one with an arbitrarily assigned value." Applicant believes that the

same arguments presented in conjunction with the response associated with claims 9-11 apply equally here. In particular, Applicant believes that, not only is there no motivation to combine IEEE 1164-1993 and IEEE 1364-1995, but there is a motivation away from combining these references. Further, IEEE 1364-1995 and IEEE 1164-1993, either singularly or in combination, do not teach or suggest all the features of claims 34 and 35, particularly the arrangement of the features in these claims.

Also regarding claim 34, on page 25 of the Office Action, the previous official notice regarding that ". . . [i]n addition, it sometimes takes time for a circuit to get defined inputs from its input circuits" was supported by citing Raimi et al., U.S. Patent 5,680,332. Applicant believes that there is no motivation to combine IEEE 1364-1995 and Raimi et al.. Still further, IEEE 1364-1995 and Raimi et al., either singularly or in combination, do not teach or suggest all the features of claim 34, particularly the arrangement of the features in these claims.

For the reasons given above, Applicant believes that claims 34 and 35 are in a condition for allowance, and respectfully requests that the Examiner reconsider and withdraw the rejection of claims 34 and 35.

Support for Amendments

Support for the amendments to claims 1, 8, 15, 20, 24, 31, 32, 33, and 34 may be found in Figures 4 and 8, and the associated text (p. 8, lines 5-27 and page 10 line 7 through page 11, line 16, respectively). No new matter is introduced as a result of these amendments.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney, Sherry W. Schumm, at (480) 657-3766 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date Nov. 22, 2004

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 22 day of November, 2004.

Tina Kohut
Name

Signature